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Atty. Dkt. No. 040373-0287

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yasuyuki MORISHITA

Title: SEMICONDUCTOR DEVICE

Appl. No.: 09/621,614

Filing Date: 07/21/00

Examiner: Nadav, Ori

Art Unit: 2811

AMENDMENT AND REQUEST FOR RECONSIDERATION UNDER 37 C.F.R. § 1.116

Commissioner for Patents
Box Non-Fee Amendment
Washington, D.C. 20231

Sir:

In reply to the Office Action dated March 14, 2002, please amend the above-identified application as follows:

In the Claims:

1. (Twice Amended) A semiconductor device having an input/output protection circuit section on a semiconductor substrate, wherein:

said input/output protection circuit section comprises a plurality of field effect transistors connected in parallel, each of which has a first diffusion layer of a first conductive type and a second diffusion layer of the first conductive type and a gate electrode that is disposed between said first and second diffusion layers;

a dopant diffusion region of a second conductive type that is set at a distance from said plurality of field effect transistors;

wherein said dopant diffusion region is connected to a reference potential, and wherein the second diffusion layer is connected to an input/output terminal section;

wherein under the first diffusion layer, there is formed a first conductive type well with a lower dopant concentration than the first diffusion layer; and